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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/668,320	09/22/2000	Charles Jay Alpert	AUS920000349US1	1327

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EXAMINER	
ROSALES HANNER, MORELLA I	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 08/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/668,320	ALPERT ET AL.	
	Examiner	Art Unit	
	Morella I Rosales-Hanner	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 September 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. **Claims 1 – 21** have been examined and are pending.

Drawings

2. Figures 1A and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Information Disclosure Statement

3. The information disclosure statements (IDS) submitted on September 22nd, 2000 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement has been considered by the examiner.

4. The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A (1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered. Specifically, the specification references **[Pg 5, lines 1 – 6]** the following publications:

- Kahng and S. Muddu, "Two-pole Analysis of Interconnection trees," Proceedings IEEE Multi-Chip Module Conference, Santa Cruz, February 1995, pp. 105-110

- A. B. Kahng and S. Muddu, "A General Methodology for Responses and Delay Computations in VSLI Interconnects," UCLA CS Dept. TR-940015, 1994.

Specification

5. The attempt to incorporate subject matter into this application **[Pg 15, lines 5 – 8]** by reference to the following publications:

- P. R. O'Brien, et al., "Modeling the Driving point Characteristic of Resistive Interconnect for Accurate Delay Estimation," IEEE/ACM ICCAD, 1989, pp. 512-515.

Is improper because in any application which is to issue as a U.S. patent, essential material may not be incorporated by reference to (1) patents or applications published by foreign countries or a regional patent office, (2) **non-patent publications**, (3) a U.S. patent or application which itself incorporates "essential material" by reference, or (4) a foreign application.

6. Mere reference to the following **publications:**

- Kahng and S. Muddu, "Two-pole Analysis of Interconnection trees," Proceedings IEEE Multi-Chip Module Conference, Santa Cruz, February 1995, pp. 105-110 **[Pg 5, lines 1 – 3]**
- A. B. Kahng and S. Muddu, "A General Methodology for Responses and Delay Computations in VSLI Interconnects," UCLA CS Dept. TR-940015, 1994 **[Pg 5, lines 3 – 6]**
- L. T. Pillage and R. A. Rohrer, "Asymptotic Waveform Evaluation for Timing Analysis," IEEE TOAD, 9(4), 352-366, 1990 **[Pg 5, lines 8 – 10]**
- Tutuianu et al., "Explicit RC-Circuit Delay Approximation Based on the First Three Moments of the Impulse Response," IEEE/ACM DAC, 1996, pp. 611-616 **[Pg 11, lines 26 – 29]**
- Kay and Pileggi, "PRIMO: Probability Interpretation of Moments for Delay Calculation," IEEE/ACM design Automation Conference, 1998, pp. 463-468 **[Pg 12, lines 1 - 4]**
- Lin et al., "h-gamma: An RC Delay Metric Based on a Gamma Distribution Approximation to the Homogeneous Response," IEEE/ACM ICCAD, pp. 19-25 **[Pg 11, lines 26 – 29]**

Is not an incorporation of anything therein into the application containing such reference for the purpose of the disclosure required by 35 U.S.C. 112, first paragraph. In re de Seversky, 474 F.2d 671, 177 USPQ 144 (CCPA 1973).

Claim Rejections - 35 USC § 102

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7.1 **Claims 1 – 5, 8 –12 and 15 –19** are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No 6,347,393 issued to Alpert et al, hereafter referred to as *Alpert*.

The applied reference has a common Assignee and two common Inventors with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventors of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

7.1.1 As regard to **claims 1, 8 and 15**, *Alpert* teaches **[Col 10, lines 1 - 20]** utilizing a signal delay model for determining an interconnect delay at a node in an interconnect having a plurality of nodes, said method comprising:

- determining an equivalent effective capacitance value for a downstream load seen at said node; and

- utilizing said equivalent effective capacitance value to calculate said interconnect delay at said node.

7.1.2 As regard to **claims 2, 9 and 16**, *Alpert* teaches [**Col. 10, lines 17 - 18**] performing a bottom-up tree traversal to compute the first three admittance moments for each of said plurality of nodes in said interconnect.

7.1.3 As regard to **claims 3, 10 and 17**, *Alpert* teaches [**Col. 10, lines 17 - 18**] determining an equivalent effective capacitance value by determining interconnect delays for nodes in said interconnect preceding said node.

7.1.4 As regard to **claims 4, 11 and 18**, *Alpert* teaches [**Col. 10, lines 12 - 26**] determining an equivalent effective capacitance by utilizing a pi-model to model said downstream load.

7.1.5 As regard to **claims 5, 12 and 19**, *Alpert* teaches [**Col. 10, lines 19 -26**] determining an equivalent effective capacitance by determining an Elmore delay value (as part of the Van Ginneken's algorithm) for said node.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8.1 **Claims 6, 7, 13, 14, 20, and 21** rejected under 35 U.S.C. 103(a) as being obvious over **US Patent No. 6,347,393** issued to Alpert et al as applied above in view of a printed publication by Qian et al. titled "Modeling the "Effective Capacitance" for the RC Interconnect of CMOS Gates", hereafter referred to as *Qian*.

The applied reference has common inventors and assigned with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). For applications filed on or after November 29, 1999, this rejection might also be overcome by showing that the subject matter of the reference and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person. See MPEP § 706.02(l)(1) and § 706.02(l)(2).

8.1.1 As regard to **claim 6, 13 and 20**, *Alpert* teaches **[Col. 10, lines 15 - 27]** an equivalent effective Capacitance (Ceff) that is characterized using the technique disclosed by Qian et al., "Modeling the "Effective Capacitance" for RC Interconnect of CMOS Gates".

Alpert does not expressly teach an equivalent effective Capacitance (Ceff) that is characterized by:

$$Ceff = Cfj\ (1 - e^{-T/tdj})$$

Wherein Cfj, is the far-end capacitance of said pi-model at said node, T is the Elmore delay at said node and tdj is the resistance of said pi-model (Rdj,) multiplied by Cfj.

Qian teaches **[Pg 1530, left Col]** a characterization of the effective capacitance that is based on the pi model, the Elmore delay and the RC interconnect which is equivalent to the characterization claimed by the inventors of the instant application. *Qian* also teaches **[Pg 1526, right Col, 1st full paragraph]** that given the RC interconnect parameters and the k-factor equations for delay and output transition time as a function of load capacitance, the delay can be calculated with reasonable accuracy.

Therefore, it would have been obvious to one of ordinary skills in the art, at the time of the invention, to substitute the Applicants' characterization of the effective capacitance for the effective capacitance characterization as taught by *Qian* in order to calculate interconnect delay with reasonable accuracy.

8.1.2 As regard to **claim 7, 14 and 21**, *Alpert* teaches **[Col. 7, lines 58 - 67]** a delay model that is characterized as:

Delay(v)=K.sub.v +R.sub.v C.sub.T(v)

Wherein:

v is the point where the delay is being calculated,

K.sub.v is the intrinsic delay at that point,

R.sub.v is the intrinsic resistance at that point, and

C.sub.T(v) is the lump capacitance

Alpert does not expressly teach a delay model that is characterized by:

$$ECMj = ECMp(j) + Rj\ (Cj + Cnj + Cfj\ (1 - e^{-T/tdj}\ ))$$

Wherein:

ECMp(j) is the computed ECM delay at the node immediately preceding said node,

Rj is the resistance between said node and said preceding node,

Ci is the capacitance to ground at said node and

Cnj is the near-end capacitance of said pi-model at said node.

Qian teaches **[Pg 1526, right Col]** that one difficulty with the effective capacitance model is that while it predicts the gate delay with reasonable accuracy it is very difficult to even specify the signal transition time since the RC shielding effects give the signal a strong nonlinear character. *Qian* further teaches **[Pg 1528, right Col, last paragraph - Pg 1529, left Col]** that while a single capacitance value seems to result in a delay close to that obtained using the pi model load, it is impossible to capture both the delay and the output waveshape with a single capacitance value overcome the previously stated difficulty with popular effective capacitance models.

It would have been obvious to one of ordinary skills in the art, at the time of the invention, to modify the delay model taught by *Alpert* and come up with a delay that takes into account the different capacitances involve in determining an interconnect

delay in an interconnect having multiple nodes as taught by *Qian* in order to capture a delay model that overcomes the shortcomings of popular models as also taught by *Qian*.

Additional references

9. The following is a list of references that are relevant to the claimed invention but were not cited by the examiner:

- Curtis L. Ratzlaff, Satyamurthy Pullela and Lawrence T. Pillage, "Modeling the RC-Interconnect Effects in a Hierarchical Timing Analyzer", IEEE 1992 Custom Integrated Circuits Conference, Pgs 15.6.1 – 15.6.4.
- Andrew B. Kahng and Sudhakar Muddu, "Two-pole Analysis of Interconnection Trees", 1994 IEEE, Pgs 105 – 110.
- Charles J. Alpert, Anirudh Devgan and Stephen T. Quay, "Buffer Insertion with Accurate Gate and Interconnect Delay Computation", DAC '99, Pgs 479 – 484
- Charles J. Alpert, Anirudh Devgan and Stephen T. Quay, "Buffer Insertion for Noise and Delay Optimization", IEEE transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol 18, No.11, Nov 1999, Pgs 1633 – 1645

10. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Morella Rosales-Hanner whose telephone number is (703) 305-8883. The examiner can normally be reached Monday-Friday from 7:00 a.m. to 3:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can be reached on 703 308-6647. The fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

MRH

Aug 19th, 2004